DESIGN OF A LOW NOISE, LOW POWER AND SPURIOUS FREE PHASE FREQUENCY DETECTOR AND CHARGE PUMP FOR PHASE-LOCKED LOOPS

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ABSTRACT

This paper presents a very simple approach to design effective PFD (Phase Frequency Detector) and charge pump (CP)circuitsfor high frequency Phase-Locked Loop (PLL) applications. ThePFD design uses only six transistors for the detection process, which reduces the chip area and power consumption of the PLL block. It also minimizes the dead zone and eliminates the reset path to reduce the delay. The output is passed through a buffer to suppress the distortion and to reduce the overall output noise. Phase noise has been reduced to -156 (dBc/Hz) at 1 MHz offset frequency. A simple current mirror based charge pump circuit is presented next. The charge pump design incorporates the use of transmission gates and transistors as capacitors to reduce switching error and clock feed through. The proposed design has a symmetric structure in terms of W/L ratios,transistor positioning and number of transistors in both up and down network, which produces a stable charging operation and reduces the spurious jumps in the output voltage. The overall output noise including thermal and flicker noise of the complete design at high frequencies is as low as -213 db at 4GHz. The proposed design provides ahigh output voltage swing of 1.4V while operating at 1.5V supply voltage. The design has been implemented in 1P-9M UMC 90nm CMOS technology. Simulations show the effectiveness of the design in terms of lower power consumption, lower noise and reduced distortion.

Key Words: *Phase Frequency Detector, Charge pump, Phase Locked Loop,Low noise, Low Power.*

INTRODUCTION

Phase-locked loops (PLL) play a critical role in a number of analog and digital radio frequency systems, computer systems, clock generation and other communication systems[1,2]. The basic building blocks for a generic PLL are the phase frequency detector (PFD) and charge pump (CP). The phase-locked loops (PLLs) based on charge pumps are used in many applications systems because of their high speed, low level of complexity and symmetric design[3].

This type of PLL often has a PFD as the first block to check the difference of phase and frequency between in reference signal and the internal voltage controlled oscillator (VCO) signal. Charge pump converts the pulses generated by PFD into a voltage signal, which is then fed to drive the VCO. The design of PFD largely determines the characteristics of PLL because the efficiency of feedback is determined by the fact that how accurate and fast a PFD can detect the difference. While designing the charge pump and PFD, many issues arise like dead zone, timing and current mismatch, overlap capacitances and reset path delays. Another major and most important issue is the phase noise added by these two blocks. All these important design issues have been discussed in section 3 of this paper.

Conventional Charge Pump and PFD

The conventional charge pump with a phase frequency detector is shown in Fig.1. The operation of this circuit is very simple. The D-Flip flop will generate the UP or DN signal depending upon the rising edge of REF or VCO_{out} signal.Either PFD will generate UP or DN signal which switches the charge pump current. If UP is high and DN is low then I_{UP} will charge the capacitor. If UP is low and DN is high then I_{DN} will discharge the capacitor. In case if both are low, then both switches will remain off providing a constant level of voltage at the output.

Although the conventional design performs the desired operation but it still has many imperfections including timing mismatches, reset path delay and dead zone in PFD. Moreover the charge pump non-idealities include the current mismatches between UP and DN networks, charge injection when MOS switches change their state and low output voltage swing. Transistors also suffer from the thermal noise for the time it remains in the ON

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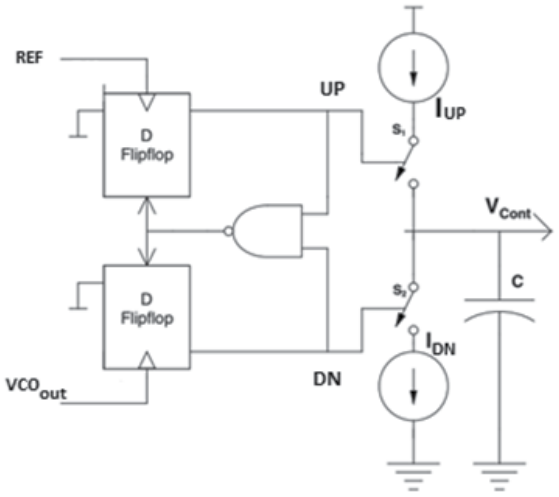

Fig 1: Conventional Design of PFD and CP

state and switching of transistor induces flicker noise. These issues call upon for a PLL topology to get the results with lesser non-idealities.

Previous Work

An efficient design with less non-ideality is presented in[3], giving high lock range and very less locking time but it also requires large are and power consumption. Methods for phase noise modeling and its reduction in PFDs and Charge pumps is given in[4-8]. A PFD design had been proposed in[9] with minimum blind zone but it uses more number of transistors which increases the power consumption. The other PFD designs reported in[10-12] are used especially for operations of PLLs at high frequencies. However, the design presented in[10] has large reset path delay, which would induce timing mismatches in charge pumps. Design of charge pump presented in[13,14] have reduced current mismatches giving better results but at the cost of chip area and power consumption as they utilizes large number of transistors. In[15], a modified version of D-flip flop is introduced which helped in making a dead zone free PFD. The major issue in that design is that it only gives dead zone free result up to 200MHz. It has dead zone of 80ps at 600MHz and it increases with the increase in frequency. Moreover, both designs discussed above had not offered any solution to reset path issue. In[16] a design with less dead zone is presented and it also eliminates the reset path but its output is not smooth and contains spurious peaks, which would later on affect the charging phenomenon of charge pump. In[17] a charge pump with high output voltage swing is presented which helps to utilize maximum tuning range of VCO and hence increases the PLL lock range but it also have high power consumption. This paper presents the PFD and CP design with the following design contributions. Because of the addition of buffer in the proposed PFD, it gives low output noise and very smooth response without glitches. The proposed PFD eliminates the reset path of a conventional PFD and hence reduces the delay and timing mismatches encountered in conventional PFDs. Addition of transmission gates also helps in reducing the timing mismatches. Placement of switches near the supply rail and addition of MOS capacitors between switches and the charge pump reduces the charge injection and clock feed through. The use of similar ratio transistors for the symmetric Charge Pump (CP) design helps to reduce the current mismatches. The design also produces high output swing voltage, which helps to utilize full tuning range of VCO. As compared to the other recently reported designs, the proposed design induces lesser noise and consumes lesser power even at higher offset frequencies.

Design Considerations

As mentioned above that while designing the PFD and CP, many parameters and non-idealities must be taken into account for a close to ideal design. The major issues in PFD are the dead zone, high power consumption when operating at high frequency, low maximum-detectable-frequency and too many transistors increasing the area. Dead zone can be defined as the minimum pulse width required for turning on the charge pump completely. The phase error cannot be detected properly if PFD is operating in dead zone. Fig.2 shows the phase characteristics of PFD with and without dead zone.

Another major drawback of conventional PFD is the reset path delay.If the delay is too long to reset the pulses, wrong polarity may be induced in the output of the PFD, which eventually leads to the wrong output of the charge pump.

After ideal phase detection, noise cancellation is another important design consideration of this system. We have seen that due to the thermal and switching noise of transistors, some unwanted peaks appear in the output waveform of PFD. This signal is fed to the charge pump, which is responsible for the output voltage, and current, which is proportional to the phase difference.

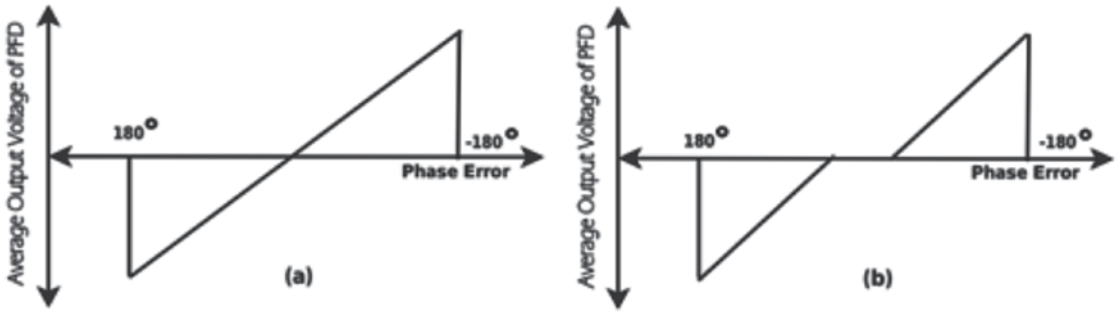

Fig 2: Output voltage VS phase error (a) No dead zone (b) Dead zone at origin

The output current I_{CP} is dependent on the phase difference Φ described by equation (1) in[4]. Taking all the non-idealities in consideration we can write as

$$I_{CP} = \Phi K_{PD}\left(1 + \frac{\beta}{2}\Phi\right) \quad (1)$$

where β represents the first order non-linearity in the system. It is evident now that any non-linearity, fluctuation, noise or distortion will ultimately result in the disturbance of charge pump current. Usually the noise increases as we increase the operating frequency.

In the conventional charge pump design, the major issues are the timing mismatch, current mismatch, charge injection, charge sharing and clock feed through. Although we cannot fully eliminate all of the non-idealities but we can strive for an optimum design offering the acceptable results with minimum non-idealities. The major cause of mismatch is the mismatch of transistors. The UP and DN currents are usually implemented by N-type and P-type current mirrors. The difference of MOS transistors results in the *current mismatch*, which occurs in charging and discharging of the capacitor of the loop filter. The UP switch is operated by the inverted input because of the presence of the PMOS transistor, so an extra inverter in needed. The delay of the inverter is responsible for the *timing mismatch* which means different arrival time of pulse at UP and DN switches. *Leakage current* is another factor, which affects the output voltage in loop filter[18]. Non-ideal behavior of switches implemented with MOSFETS, increases charge injection and clock feed through. The total error because of the non-idealities can be summed up in[5] as

$$\Delta\Phi_{tot} = \Delta\Phi_{leak} + \Delta\Phi_{mismatch} + \Delta\Phi_{timing}$$
$$= 2\pi\left\{\frac{I_{leak}}{I_{cp}} + \frac{\Delta_i}{I_{cp}}\frac{t_{on}}{T_{ref}} + \frac{\Delta t_{delay}}{T_{ref}^{\ 2}}t_{on}\right\} \quad (2)$$

In the above equation, I_{cp} is the current rating of charge pump, I_{teak} is the leakage current, T_{ref} is reference cycle time, t_{on} is the turn ON time of PFD whereas Δ_i and Δt_{dealy} are the mismatch of current and timing respectively. To minimize the error we have to minimize leakage current I_{teak}, mismatch current Δ_i and timing delay Δt_{delay}. The delay can be minimized by reducing the logical delay between output of PFD and CP switches[5].

The main reasons of mismatches are described above whereas the main sources of leakage current are *charge injection, charge sharing* and *clock feed through.* Switching transistors carry some charge in their layers and they disperse this charge into load capacitance through drain terminal in switching OFF process. This *charge injection* results in the unwanted spikes in output voltage. *Charge sharing* is the phenomenon, which occurs during the switching ON process. The floating output voltage of the charge pump share the charge when the transistor turns ON through parasitic capacitance of the charge pump, resulting in some deviation or attenuation of the output voltage[18].

Both the above described charge issues are because of switches and this charge can be expressed in[8] as

$$\left|Q_{CH}\right| = WLC_{ox}V_{ov} \quad (3)$$

Usually the switches have different W/L ratios and different overdrive voltages, so they do not cancel each other's charge and this charge disturbs the control voltage. Another factor that affects the performance and output voltage is the *clock feed through*. This is because UP and DN pulses couple through the gate drain capacitances to reach on output voltage node[8].

An important design factor in this design is the

locking range of PLL, which is dependent on the *output voltage swing*. The output voltage of loop filter, which is the control voltage, should provide maximum swing (ideally rail to rail) in order to utilize the full tuning range of VCO[18]. Therefore, this parameter is very critical and performance of charge pump is directly related to this factor.

Charge injection and clock feed through also result in low output voltage swing. Secondly, the gate-drain overlap capacitances also attenuate the output voltage by some factor. This attenuation is given in[8] as

$$\Delta V = \frac{C_{GD1} - C_{GD2}}{C_{GD1} + C_{GD2} + C_1}\left(V_{DD}\right) \quad (4)$$

Where and are capacitances of PMOS and NMOS switches and C_1 is the capacitor of loop filter. These capacitances attenuate the output voltage swing of charge pump.

After considering all the design parameters, the output noise and phase noise must also be considered in order to get close to ideal design. MOS transistors introduce various noises during switching transition and during the time in which they remain in the ON state. In[7] the complete noise analysis of MOS transistors and of two major topologies to realize the PFD is carried out. First is using static NAND gates, and the other one is employing true single-phase clocking (TSPC). Both topologies induce noise in the system. In this paper, the later one is used with some other amendments. This is because the overall noise of NAND gate based PFD is large as it uses greater number of transistors.

The noise analysis of CMOS inverter will also help in understanding the noise issues in PFD. A CMOS inverter and its noise waveforms are shown in Fig.3.

The transistors inject the flicker and thermal noise when they turn ON. The flicker noise pulsates only during transition time while thermal noise envelope remains for the time the transistor remains ON. Now to reduce the flicker noise we can increase either the length or width of the transistor. However, the long channel devices raise the time ΔT, which in the ON state time of transistor and the phase noise is directly dependent on the ΔT[7]. Therefore, to reduce the flicker noise we must use the wider devices.

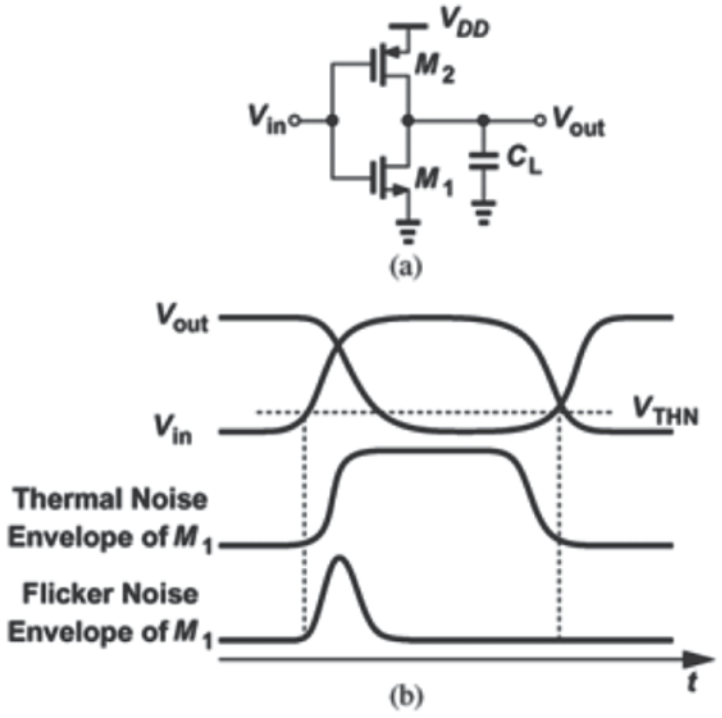

Fig 3: (a) CMOS Inverter (b) Thermal and flicker noise

Both thermal and flicker noise are responsible for increase in phase noise. Therefore, to reduce phase noise a common approach is to increase the width of transistors but this will increase area and power consumption. Design optimization in[7] focuses separately on the widths of *driver* transistor W_a and that of driven transistor W_b. The driver transistor is responsible for switching and a driven transistor is responsible for current in the design. The capacitance of output node C_L is proportional to the total width of both transistors. The phase noise in this case is given in[7] as

$$S_{\Phi}(f) \propto \frac{f_{in^2} V_{DD^2} C_{L^2}}{W_{a^3}} \left(\frac{1}{f}\right) \quad (5)$$

In above equation $\frac{1}{f}$ is the drain noise current spectrum, f_{in} is the input frequency and V_{DD} is the supply voltage. So in order to get the optimum design, the width of driver transistors is kept low and that of driven transistors is high.

Proposed Design

Design of Phase Frequency Detector(PFD)

A simple, symmetric, distortion free PFD is shown in Fig.4 and complete design with spurious-jumps free charge pump with improved current mismatches, less non-idealities and reduced switching errors is shown in Fig.4. The proposed PFD design uses only six transistors to detect the phase and frequency difference. It also eliminates the reset path of conventional PFD and hence reduces the delay and timing mismatches. M1-M3 are used to construct the Up network while M4-M6 form is the down network of the proposed PFD. Principle of operation is very simple. A rising edge on the reference signal turns ON the M2, M6, and thereby forcing the UP signal to a high state. The rising edge on VCO signal turns ON the M5 and M3 and hence gives a high state to DOWN signal. In case if both signals are at high state, the transistors M3 and M6 pull down both signals to zero logic state without any reset delay.

The obtained waveform still has some noise and distortion content which would later on affect the smooth charging of the charge pump. The distortion can be reduced using different techniques, but as we focus upon a high frequency design, so we must add such components, which do not add more noise at higher frequencies. In this design, buffer is utilized to remove glitches and non-idealities from the waveform.This *buffer* is realized by combining two *CMOS inverters* and output of the first is fed to the input of second inverter. An inverter gives the output when the input signal crosses the threshold level. In this way, it removes those small

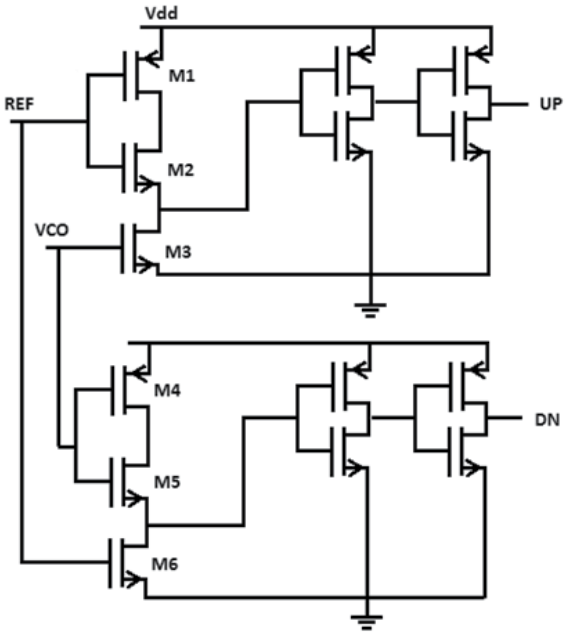

Fig4: Proposed design of Phase Frequency Detector(PFD)

noise components and distortions, which appear in the output even when PFD output is at OFF state. The buffer uses the same level of supply voltage as PFD. This restricts the maximum output level and hence clips off the unwanted abnormal peaks from the output waveform of PFD. A very similar approach is used in the DN (down) network. Simulation results show that this not only reduces the abnormal peaks in the output waveform but it also reduce the noise significantly.

Design of Charge Pump

The various non-idealities associated with the charge pump design are discussed in section 3. We shall now address them one by one in this section. In the design shown in Fig.5(a), the switches of charge pump are realized by using M9 and M10 operated by complement of UP and DN signals. These signals from PFD may arrive at different times because one is passed through one inverter and the other is passed through a buffer. This creates a timing mismatch and can add up in phase error. To remove *the timing mismatch,* transmission gates are inserted in both UP and DN networks to replicate the delay of the inverter. The use of two different current mirrors could produce some *current mismatch* at the output node as well. To avoid this situation, the W/L ratio of both mirrors is kept the same.

Charge sharing and *charge injection* are the problems associated with the ON and OFF switching process

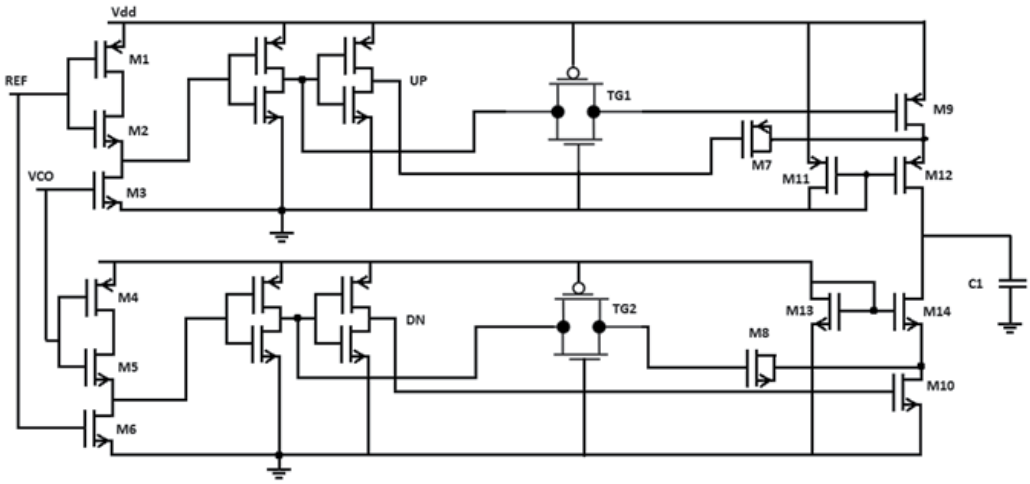

Fig 5(a): Complete Schematic of the proposed PFD and Charge pump Circuit

while *clock feed through* is because of the coupling of pulses through gate drain capacitances. Two techniques are used to minimize these effects. First is to place the switches near the supply rails to reduce the feed through by the total capacitance seen from the drain terminal of the switches to ground before disturbing the source voltage of M12 and M14. Secondly, additional transistors are added between switches and charge pumps. These transistors M7 and M8 are used as capacitors and they are driven by the complemented signal in comparison with the signal applied to switches. Clock feed through of each switch is cancelled be setting $W_7 = 0.5\ W_9$ and $W_8 = 0.5\ W_{10}$. These transistors remove the effect of charge injection and clock feed through, and the result is a smooth charging phenomenon. The choice of W/L ratio is of critical importance here because this ratio gives the value of capacitance offered by the transistors.

To get the inverted signal, the intermediate stage of the buffer is used. The use of an inverted signal causes a timing delay in the signal and hence produces non-idealities and timing mismatches. This is the main reason of *slow-node* problem and glitches in the output of charge pump. To counter the effect of this delay, transmission gates TG1 and TG2 are inserted which add to the delay in non-inverted signal as well.

The W/L ratio of these gates is equal to that of the invertors to produce the same delay. At the end of the charge pump, loop filter minimizes the ripples in output

voltage. The overall design of the structure is kept very symmetric and W/L ratios are chosen in such a way to reduce the turn on , turn off and reset time, minimize the non-idealities, maximize the output voltage swing, reduce the slow node issue, rectify the glitches in output and to ensure the smooth operation. All the ratios are in Table 1.

SIMULATION RESULTS

The proposed topology is designed in Cadence Virtuoso using UMC's 90nm 1P9M Logic/Mixed Mode Low-K SP Process . UMC 90nm offers raw gate density of 400,000 gates/mm2 and also offers high density needed for low cost applications. It has a complete set of models for industry-standard EDA tools like Cadence

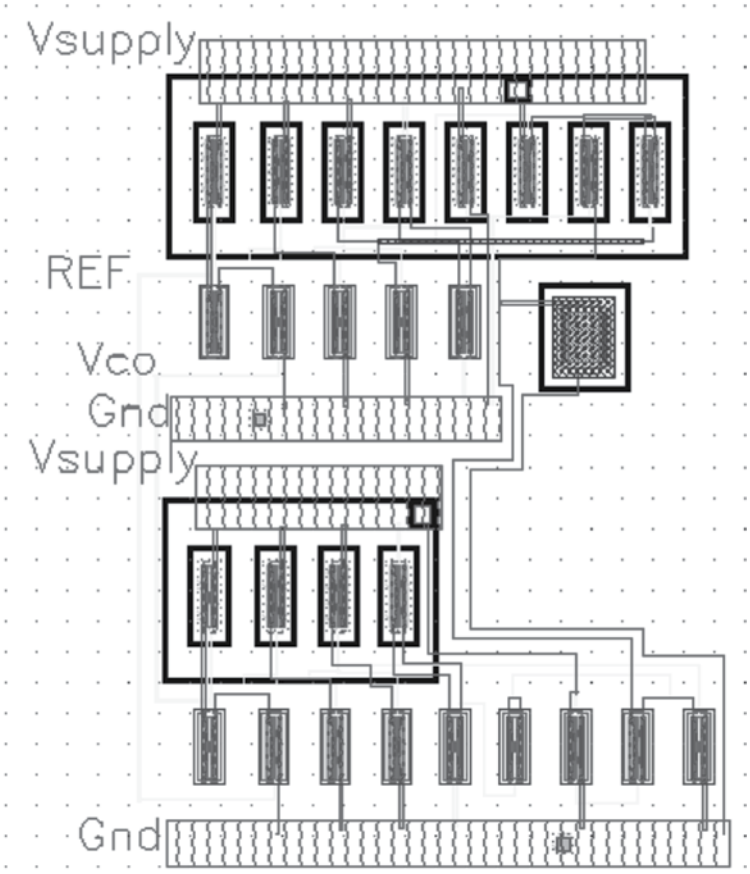

Fig 5(b): Complete Layout of the proposedPFD and Charge pump Circuit in UMC 90nm CMOS

virtuoso. It has full set of gated clock buffers for power saving. The complete analysis of the proposed design is performed in Cadence Virtuoso using a 2V supply voltage. The layout of the circuit is in Fig. 5(b). The analysis results are in this section.

Transient response of PFD

The transient response is observed in case of reference signal leading the VCO signal. The response of proposed PFD is linear and without any dead zone near origin. Transfer characteristics are shown in Fig.6 and power consumption with respect to offset frequency is shown in Fig.7. We can see that the power consumption is low for higher frequencies and this makes the design suitable for high frequency applications.

Timing diagram is shown in Fig. 8. This response is without using the buffer. We can see that its operation is well in accordance with the conventional PFD. The output is better than the conventional design but it still has some glitches in it. Red circles show the glitches

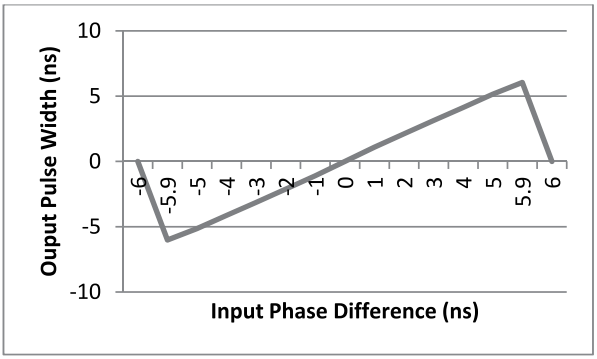

Fig 6: Phase Transfer Characteristics

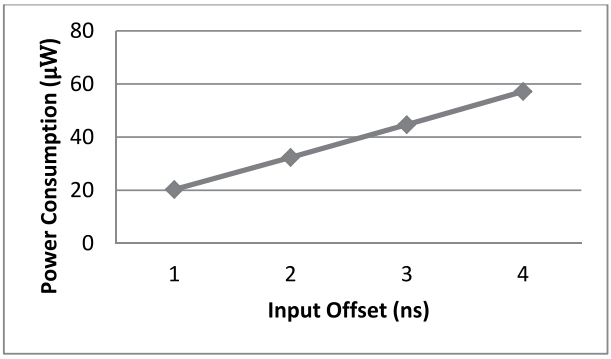

Fig 7. Power Consumption at different offset Frequency

in the output of PFD.

As mentioned earlier that these non-uniform voltage levels also appear at the output of the charge pump if we feed it, as it is, to the next block. To get a relatively smooth response, it is passed through a buffer. The improved response is shown in Fig.9. Now the output waveform is showing a smooth response of PFD as compared to previous results.

Transient response of Charge Pump

The output of PFD pass through an inverter and then through the transmission gates to match the timing and then it drives the switches of the charge pump. A charge pump has to convert the logical output of PFD

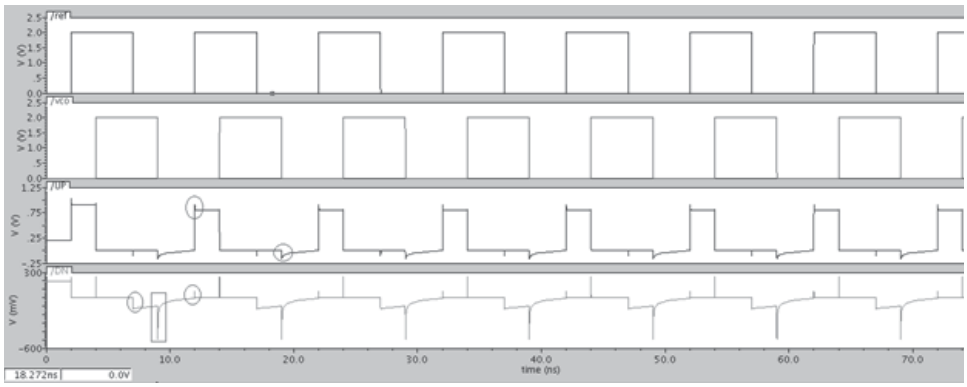

Fig 8: Simulation of PFD without Buffer

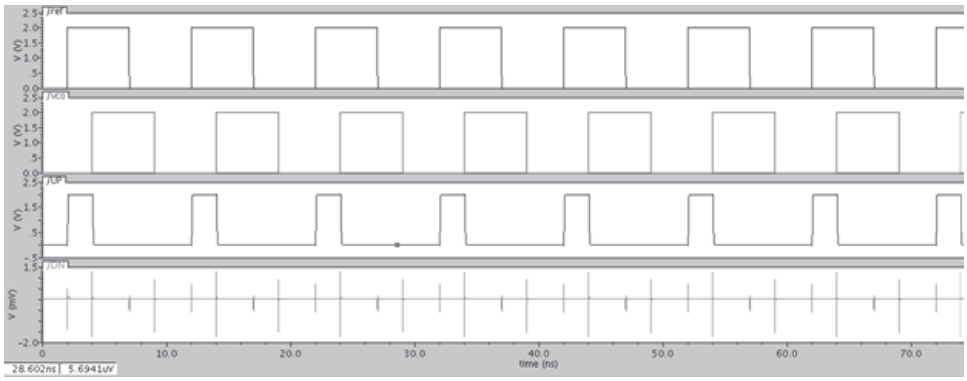

Fig9: Simulation of PFD after buffer addition

into voltage swing, which would drive the VCO for PLL applications. In our proposed charge pump, the current I_{UP} is controlled by M9, which is operated by the inverted UP signal. I_{DN} is controlled by M10 which is operated from the output of the buffer i.e. DN signal. The inverted UP signal is taken from intermediate stage of buffer and hence it has less delay as compared to the DN signal. To match the delays, a transmission gate with same W/L ratio is inserted in the path of the UP signal.

Charge injection and *clock feed-through* result in attenuation of the output voltage swing. To counter the effect, transistors M7 and M8 are added. By only setting the width of these transistors, the effect can be cancelled out. M7is driven by UP signal while M8 is operated by inverted DN signal. A very similar approach as described above is used in this case as well to match the timing delays of both inverted and non-inverted signals. The charging operation of proposed charge pump is verified in

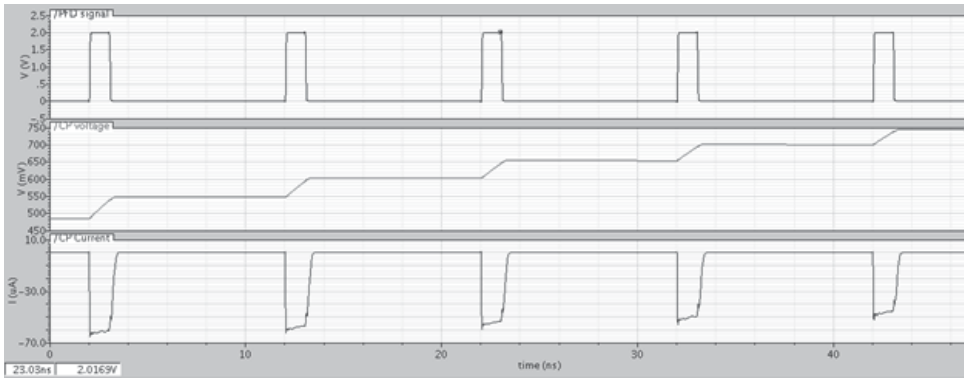

Fig 10: Simulation of Charging up operation of Charge Pump

transient response shown in Fig. 10.Reduced dead zone, less non-idealities and low noise allow operating at high frequencies as well. The above discussed design works fine up to 4GHz input frequency. Above this frequency it do not provide fine charge phenomenon. Proposed design working at 4GHz input reference frequency is shown in fig 11.

Dead Zone Analysis

As discussed in earlier sections that one ofthe important phase characteristics of PFD is dead zone because it introduces jitter in the PLL. PFD cannot properly detect the phase error in this situation and because of this, the PLL gets locked in the wrong phase and frequency. Therefore, it is very important to develop a design with minimum dead zone. The proposed design offers a minimum dead zone of 10ps at 1 GHz. The analysis is done by giving very small offset time on inputs. Two signals are provided at PFD input with only 10ps offset and simulation results are shown in Fig. 12. It is evident that the proposed PFD is efficiently detecting phase offset of even 10ps and charge pump is giving very smooth and spurious jumps free charging phenomenon. Dead zone increases with the increase in input frequency and this analysis is in Fig. 13.

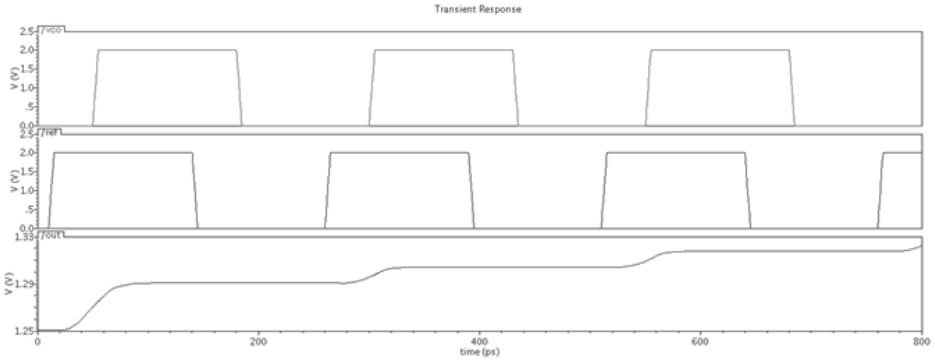

Fig 11: Simulation of Charging up operation at 4GHz input frequency

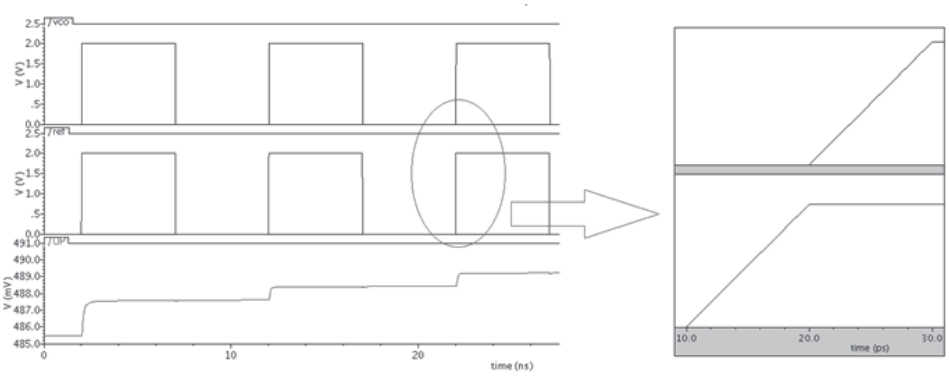

Fig 12: Dead Zone analysis of PFD

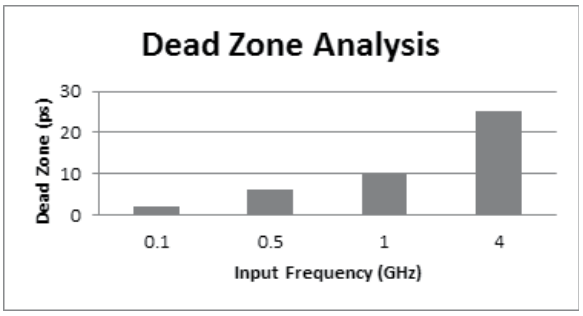

Fig 13: Dead Zone analysis of PFD at different input frequencies

Noise Analysis

As discussed in last part of design considerations section that noise issue is also a critical in design of PFDs and charge pumps. The design presented in this paper has been optimized to get minimum phase noise and overall output noise. Simulations show that the noise has been reduced significantly. The widths of transistors are adjusted according to the functionality of the transistor, in order to minimize the noise including thermal and flicker noise. Moreover, a CMOS buffer is added to reduce the distortion.

The response has been observed in Cadence Virtuoso up to 2GHz *offset* frequency. A number of designs reported recently performed comparative analysis with previous designs at 1 MHz *offset*. So in our noise response analysis, the points at 1MHz are highlighted in order to get a better comparison and to show that our design reduces the noise. Noise response without buffer is in Fig. 14 and after using buffer is in Fig. 15.It is evident now that inclusion of the buffer results in a reduced noise. We get noise reduction of almost -20dB after adding buffer.

Finally, we have to analyze the noise response of the complete design on the system and adding proposed charge pump with our improved phase frequency detector (PFD). Phase noise and the overall noise response of complete design is in Fig. 16.

The width of driver transistors (switches) are kept low while that of the driven transistors M12 and M14 are kept high in order to reduce the noise. Additional transistors configured as capacitors are added to reduce the leakage current and transmission gates are added to reduce the timing mismatches. The proposed design is suitable for high frequencies and output noise at 4GHz is -213dB as shown in Fig. 17.

Comparison with previous work

The proposed design has been compared with many other topologies configured in[9-14] where a100 MHz *input frequency* is used as a reference. So the design proposed in this paper is also analyzed at 100 MHz *input frequency*. Comparison clearly shows that our design is more efficient than the previous designs as it uses less number of transistors, consumes less power, offers minimum dead zone and it can operate up to 4GHz input frequency. Proposed design is suitable for higher frequencies and eliminates the reset path delay of PFD.The design of charge pump provides smooth charging phenomenon. To overcome the issues of non-idealities of charge pump, and to ensure smooth charging phenomenon at higher frequencies, additional transistors were required. Moreover, the design utilizes wider transistors where required. Therefore it result in a tradeoff between noise

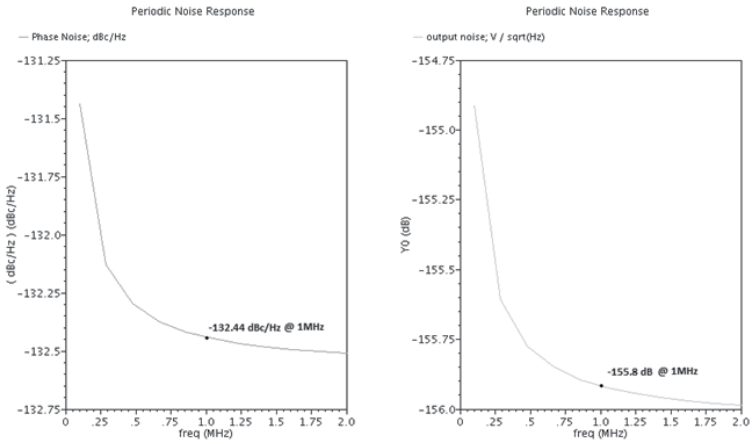

Fig 14: Noise response of PFD without buffer

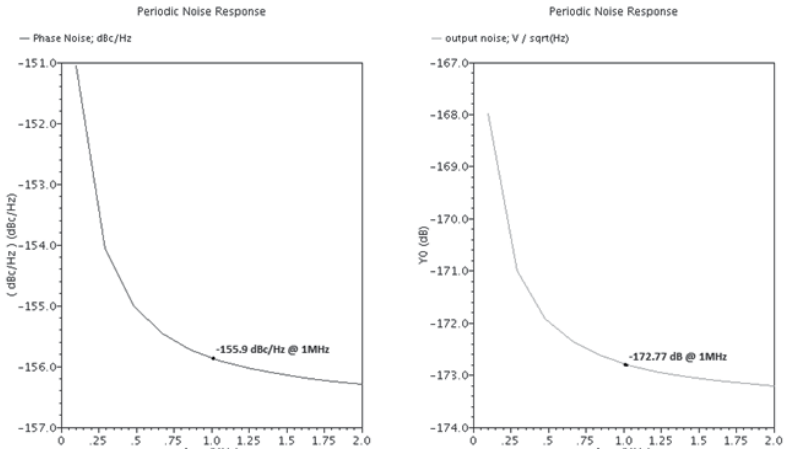

Fig 15: Noise response of PFD with buffer

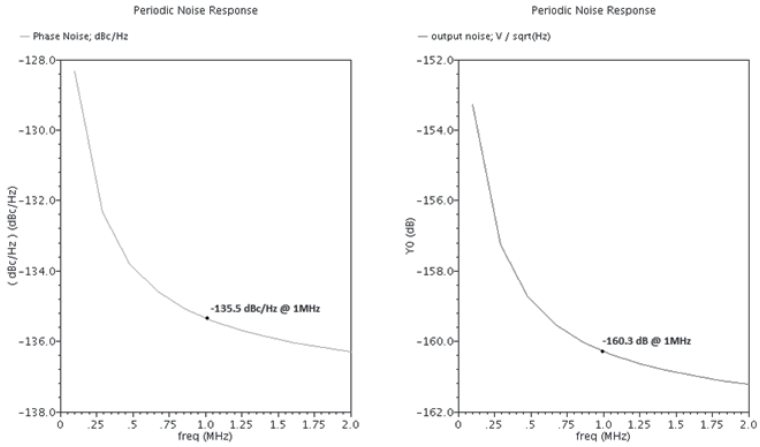

Fig 16: Noise response of Complete Design

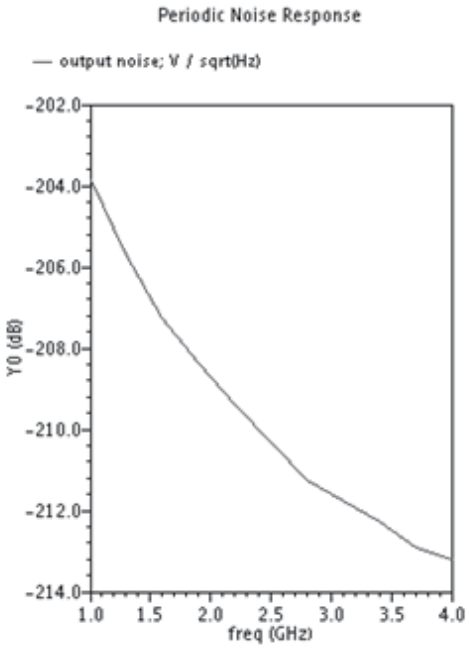

Fig 17: Noise response of Complete Design (-213 dB @ 4GHz)

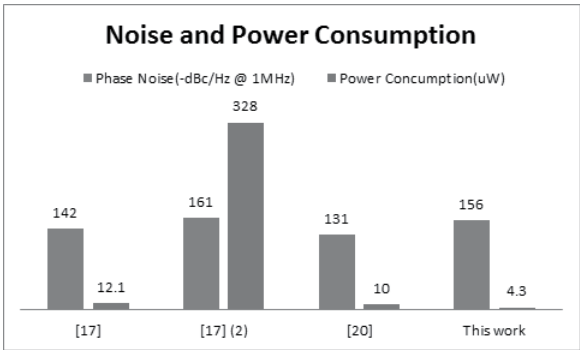

Fig 18: Noise and Power consumption comparison

and power consumption, however this increase in power is not significant. The detailed comparison of PFD and CP is in table 2 and table 3 respectively.

We can see that conventional PFD consumes a large power and has high noise. Graphical comparison of phase noise and power consumption of other research works with this work is in Fig. 18.

Conclusion and Future Work

This paper presents a high performance, phase frequency detector and charge pump for high frequency PLL applications using 1P-9M UMC 90nm CMOS process technology. Because of the addition of buffer in the proposed PFD, it gives low output noise and very smooth response without glitches. The proposed PFD eliminates the reset path of a conventional PFD and hence reduces the delay and timing mismatches. Addition of transmission gatesalso help in reducing the timing mismatches. Placement of switches near the supply rail and addition of MOS capacitors between switches and charge pump reduces the charge injection and clock feed through. Use of similar ratios of charge pumps in UP and DN networks help to reduce current mismatches. The overall design of UP and DN networks are very symmetric with respect to each other. This symmetry is in terms of placement of transistors and their aspect ratios and it reduce the non-idealities. The design also produces high output swing voltage, whichhelps to utilize full tuning range of VCO. As compared to the other recently reported designs,the proposed design induces lesser noise and consumes lesser power even at higher offset frequencies.

PLLs finds many applications in communication systems operation at high frequencies. Future era is looking forward to 5G systems. High frequency operation in such systems can lead to more signal distortion. On the other hand, proliferation of battery powered devices demands minimum power consumption. A further optimization in the design of PLL is required in future to operate at further higher frequencies with low power consumption.

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